Notice of Allowability	Application No.	Applicant(s)	
	10/696,522	VANTALON ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the application filed on 28 October 2004, and the telephonic interview on 1 December 2005*.

2. ☒ The allowed claim(s) is/are *1-7, 21-26 and 30 (as orignally filed), renumbered by Examiner (1-14)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Mr. Gregory Gulliver on 1 December 2005. The following two sets of corrections were agreed upon:

With respect to the drawings filed on 28 October 2003, the word "Figur" in Figures 7, 8 and 12 should be changed to the word "Figure".

Additionally, claims 1-6 and 21 should be changed as follows:

1. A device comprising:

a central processor and at least one coprocessor coupled to at least one bus;

a memory device coupled to the at least one bus; and

at least one register coupled to the at least one bus and including information for use in controlling at least one configuration of the memory device in response to system state information, a first configuration supporting direct access to the memory device exclusively by the at least one coprocessor, a second configuration supporting at least one of direct access to a first area of the memory device by the at least one coprocessor and indirect access

to a second area of the memory device by the central processor, and a third configuration supporting at least one of direct access to the first area of the memory device by the at least one coprocessor and direct access to a third area of the memory device by the central processor.

2. The device of claim 1, further comprising at least one decoder coupled to the at least one bus, the at least one decoder using address information on the at least one bus to select one of the memory areas to receive data corresponding to the address information.

3. The device of claim 1, further comprising at least one bridge unit that couples the at least one coprocessor and the memory device to a first bus, wherein the indirect access to the memory device by the central processor includes mapping at least one set of memory locations of the memory device through the at least one bridge unit for access by the central processor.

4. The device of claim 1, further comprising at least one memory interface that couples the memory device to a first bus, wherein the direct access to the memory device by the central processor includes mapping at least one set of memory locations of the memory device through the at least one memory interface for access by the central processor.

5. The device of claim 1, wherein the central processor is clocked at a first speed and the at least one coprocessor is clocked at a second speed.

6. The device of claim 1, wherein the at least one bus includes:

a first bus coupling the central processor to a bridge unit;

a second bus coupling the at least one bridge unit to the at least one coprocessor and the memory device.

21. A portable electronic apparatus comprising:

a central processor;

a signal processor;

a first memory area coupled for access by the central processor via a first bus;

a second memory area coupled for access by the signal processor via a second bus; and

at least one component coupled to the central processor that controls shared access to the second memory area by the central processor, the shared access including access by the signal processor and at least one of indirect access by the central processor to at least one set of memory locations of the second memory area via the second bus and direct access by the central processor to ~~the~~ a set of memory locations of the second memory area via the first bus.

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-7, 21-26, 30, drawn to a memory device (apparatus method and medium) which includes a plurality of configurations of a memory to support direct and indirect access by a plurality of processors, classified in class 711, subclass 170.

II. Claims 8-20, drawn to a system that includes a memory configured to support shared access. The address range of the data determines access to the memory, classified in class 711, subclass 147.

III. Claims 27-29, drawn to a method (and device) relocating addresses of memory based on state information, and further accessing memory based on address type information received, classified in class 711, subclass 170.

2. The inventions are distinct, each from the other because of the following reasons: Inventions I, II and III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility from inventions II and III such as use in a system to optimize access to memory (either direct or indirect) based on type of processor. Likewise, invention II has separate utility from inventions I and III, such as in a system for using the addresses, rather than processor types to determine the configuration and access of the memory unit. Finally, invention

III has separate utility from inventions I and II such as a system determine the configuration and access of a memory based on type of data. See MPEP § 806.05(d).

3. Because these inventions are distinct for the reasons given above and the search required for any one invention (i.e. invention I) is not required for either of the remaining two inventions (i.e. invention II or invention III), restriction for examination purposes as indicated is proper.

4. Applicant (Gregory Gulliver) elected Group I for examination during the telephonic interview held on 1 December 2005. Mr. Gulliver made the election of Group I without traverse, and has agreed to cancel the remaining claims.

Allowable Subject Matter

3. Claims 1-7, 21-26 and 30 are allowed.

4. The following is a statement of reasons for the indication of allowable subject matter:

As for claims 1, 22 and 30, Bays et al., hereinafter Bays (US Patent 6,965,974 B1) teaches dynamic partitioning of memory banks among multiple agents (i.e. processors). Referring to Fig. 3, a plurality of processors (elements 304, 306, 314) and super processors (elements 302 and 312) access shared memory (element 310), which is partitioned into a plurality of section (elements 310a and 310b) – col. 6, lines 18-37. The processors and super processors are connected via a system of busses (depicted in Fig. 3 which arrows which terminate at the select logic (element 312)). The configuration register (element

360) is further connected to the system in order to provide commands to select the partitioning (i.e. configuration) of the shared memory (element 310) – col. 6, lines 49-58.

Bays however fails to specifically teach configuring the shared memory into the three configurations specifically claimed by applicant including a first configuration supporting direct access to the memory device exclusively by the coprocessor, a second configuration supporting at least one of direct access to a first area of the memory device by the coprocessor and indirect access to a second area of the memory device by the central processor, and a third configuration supporting at least one of direct access to the first area of the memory device by the coprocessor and direct access to a third area of the memory device by the central processor.

As for claim 21, though Bays further teaches a signal processor accessing the shared memory (col. 7, lines 55-60), he fails to teach the indirect and direct access of the central and signal processors to each of the respective memory areas of shared memory (Fig. 3, element 310) shared access to the memory as including access by the signal processor and at least one of indirect access by the central processor to at least one set of memory locations of the second memory area via the second bus and direct access by the central processor to the set of memory locations of the second memory area via the first bus as claimed by applicant.

Claims 2-7 and 23-26 further limit claims 1 and 22 respectively therefore they too are deemed allowable.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ku (US PG Publication 2004/0158684 A1) teaches a computing system, and method for enabling a DSP to access parameter tables through a CPU.

Shelly et al. (US Patent 6006309 A) teaches information block transfer management in a multiprocessor computer system employing private caches for individual center processor units and a shared cache.

Pelelg et al. (US PG Publication 2003/0188075 A1) teaches a CPU expandability bus.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

12/5/05